Signal-based meta-modelling of temperature in short-circuit testing of power semiconductors

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Introduction

- Repetitive short circuit capability is a requirement of smart power ICs in automotive applications
- Short circuit load conditions result in a high power dissipation, temperature rise and thermal stresses
- Thermo-mechanical fatigue of the chip metallization leads to progressively degrading electrical performance and eventually failure
- Short circuit testing is done to prove meeting required quality standards and to collect data for lifetime modelling







Electro-thermal behavior of power MOSFET transistors

- In a short-circuit test, the MOSFET is operating in the so-called saturation mode, where the current is given by



When the decrease of the threshold voltage with temperature is dominant, an increase in temperature leads to an increase in current density. The increase in current density implies a local increase of power within the cell, which in turn induces a further temperature rise. This positive feedback between the current and the temperature may lead to localization of current and even thermal runaway.



Exemplary MOSFET electrical behavior



Electro-thermal FEM simulation of smart power semiconductors

 Due to the strong interaction between the electric field, temperature and current distribution, coupled electrothermal simulations are necessary to analyse short-circuit loadings



The governing equations for the temperature and electric field are

$$\rho c \frac{\partial T}{\partial t} - \nabla \cdot (\lambda \nabla T) = \vec{E} \cdot \vec{j}$$
Heat equation with Joule heating
$$\nabla \vec{j} = \nabla \cdot (\gamma \nabla \phi) = 0$$
Current continuity equation

 The electrical conductivity for the DMOS region is derived from the current density characteristic

$$\gamma = \gamma(\phi, T) = \gamma(V_{GS}, V_{DS}, T)$$



 Elements meshing the DMOS introduce a nonlocal coupling because the electrical conductivity depends on the drain- and source-side potential

$$V_{GS} = \phi_G - \phi_S$$
 $V_{DS} = \phi_D - \phi_S$



Electro-thermal FEM simulation of smart power semiconductors

... with linearized conductivity
 The DMOS conductivity is approximated with an effective conductivity, which is updated at every time step based on the field solution for each element
 The DMOS conductivity model is used with the full non-local dependence on the electric field and
 Solver: Ansys Mechanical APDL [1]
 Solver: OpenCFS [2], COMSOL Multiphysics

Given the solution $T(x, t_n), \phi(x, t_n)$ and boundary

condition $V(t_{n+1})$ and $I_d(t_{n+1})$, solve

Typical solution times depending on the model size are 1 to 6 hours

It is feasible to simulate a test series of e.g. a dozen devices in a reasonably short time. Once this computational cost has been paid sufficiently often, it is desirable to have meta-models for key properties to avoid repetitive simulations and to enable quick parametric studies

[1] de Filippis et al., ANSYS based 3D electro-thermal simulations for the evaluation of power MOSFETs robustness, Microelectronics Reliability, Volume 51, Issues 9–11, 2011

temperature

[2] Eisner et al. (2017). Finite-Element Analysis of Coupled Electro-Thermal Problems With Strong Scale Separation. IEEE Transactions on Power Electronics, 32(1), 561–570. https://doi.org/10.1109/tpel.2016.2527690



Electro-thermal FEM simulation of smart power semiconductors

- Simulation workflow
 - Device and test data are collected from a database
 - Processed simulation results are collected and stored in the database



- Meta-modelling challenge
 - The load during a short-circuit test cannot be described by a set of scalar parameters
 - The meta-modelling workflow must be able to work with input **signals** in addition to scalars



optiSLang workflow

optiSLang project for MOP creation



infineon

optiSLang workflow

- MOP creation and evaluation are conveniently done via a web application to run the optiSLang projects
- MOP workflow development version; to be linked to internal data environment using Python APIs

Interface for creating the MOP		Interface for evaluating the MOP	
Signal-In/Signal-Out Analysis		Signal-In/Signal-Out Analysis	
Create MOP	Evaluate MOP	Create MOP	Evaluate MOP
Create MOP		Evaluate MOP	
Training Dataset First training design Last training design Number of input shapes Variability fraction		MOP First training design Last training design Number of in shapes Var fraction	✓
Project settings		Evaluation Dataset First evaluation design Last evaluation design	
Project name		Project settings	
		Project name	

Designs for MOP training



- 350 designs covering various loads as well as 2 operation modes of the chip and 2 physically different variants of the interconnect layer have been used to create the DIM-GP signal MOP
- F-CoP is better than 95% in the most important time range
- Time for training was ~45 minutes on Intel Xeon workstation





Testing the MOP on new data

- MOP predictions of 613 designs that were not used for training are in very good agreement with simulated signals
- Errors measures show only a small number of designs that are approximated poorly by the MOP





Testing the MOP on new data

- The low quality predictions were obtained for signals in the time range where only a small of amount of designs was available for training
- Selection of training data was for demonstration purposes and not optimized for coverage!





Summary

- A workflow to use signals and scalar parameters as input for a metamodel has been developed and applied for the prediction of the electro-thermal behavior of a smart power switch
- Building the MOP using two input channels and two scalar parameters is as fast as performing a single electrothermal simulation
- Current limitations
 - All input signals must have a common sampling, which requires pre-processing in the case of irregularly sampled data
 - Need for dense sampling to correctly interpolate steep flanks in the signals
 - Output predictions are limited to the sampled time range

